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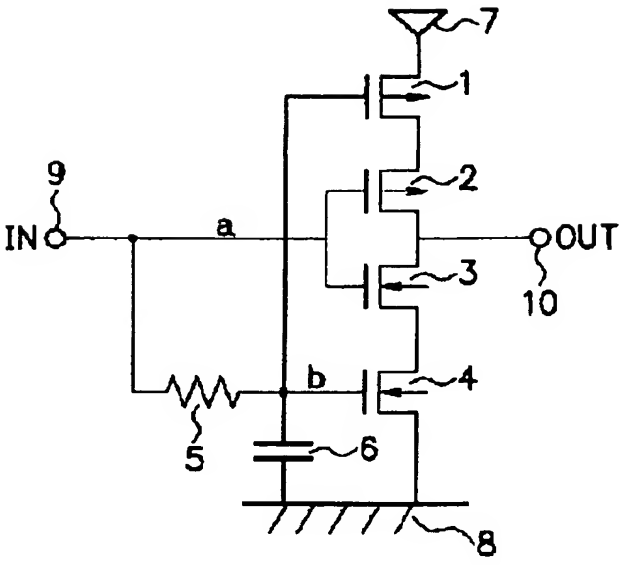
TITLE : CMOS LOGIC CIRCUIT



ABSTRACT : PROBLEM TO BE SOLVED: To obtain a CMOS logic circuit that can reduce a through-current in spite of a fewer inserted delay circuit numbers.

SOLUTION: A push-pull gate circuit consisting of P-channel transistors(TRs) 1, 2 and N-channel TRs 3, 4 and providing different ON/OFF operations to an input signal is connected in series between a power supply and a GND, and delay circuits 5, 6 delay the input signal by a prescribed time. The input signal (a) is given to any gate terminal of the push-pull gate circuit, an input signal (b) via the delay circuit is connected to other gate terminal of the push- pull gate circuit, and a connecting point of the series connection of the push-pull connection TRs 2, 3 is connected to an output signal terminal 10, and the input signal 9 is given to the output signal terminal 10. The ON/OFF operation timing of the push-pull gate circuit is made different by the delay circuit. Thus, simultaneous tuning on of the gate circuits can be prevented and the through-current can be reduced.